Notice of References Cited	Application/Control No. 09/388,766	Applicant(s)/Patent Under Reexamination SHIH ET AL.	
	Examiner Ayal I Sharon	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Smith, D. J. "VHDL & Verilog Compared & Contrasted – Plus Modeled Example Written in VHDL, Verilog and C." Proc. 33rd Design Automation Conf. June 3-7, 1996. pp.771-776.
	V	Berman, V. "Standard Verilog-VHDL Interoperability." Proc. VHDL Int'l Users Forum. May 1-4, 1994. pp.142-149.
	W	QuickLogic QuickNote #61 "Initializing Flip-flops in QuickWorks Simulations". Last Updated: 3/19/98.
	X	Maginot, S. "Evaluation Criteria of HDLs: VHDL Compared to Verilog, UDL/I, and M". Proc. EURO-DAC '92. Sept. 1992. pp.746-751.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.